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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/996,342	11/21/2001	Tohmas Eugene Waschura	WASC1821	1977

7590 07/20/2005

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EXAMINER	
LAU, TUNG S	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 07/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/996,342	WASCHURA ET AL.	
	Examiner	Art Unit	
	Tung S. Lau	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1, 7, 8, 9, 15, 16, 2, 3, 4, 5, 6, 10-14 are rejected under 35 U.S.C. 102(a) as being anticipated by Thomas Eugene, James Roger, Robert Lee (EP 1143654).

Regarding claim 1:

Thomas Eugene, James Roger, Robert Lee disclose apparatus for measuring characteristics of a bit stream of binary pulses comprising control means for defining a window comparator (abstract, fig. 2, unit 203, 200), and logic means for accumulating time and voltage event counts (Col. 4-6, section 0017-0019) of the bit stream pulses falling within voltage threshold and points inside the window comparator during durations of the binary pulse bit stream and drawing eye diagrams therefrom defining the bit stream characteristics (fig. 2, unit 200, 203, 20, 3, fig. 3, unit 21111, fig. 4, unit 21120).

Regarding claim 7:

Thomas Eugene, James Roger, Robert Lee disclose apparatus for measuring characteristics of a bit stream of binary pulses comprising control means for

defining a window comparator of an array of columns and rows defining points for accumulating voltage counts of the binary pulse bit stream at time offsets during defined durations of the binary pulse bit stream (abstract, fig. 2, unit 203, 200), and apparatus for creating a voltage threshold window that moves between minimum and a maximum voltage levels (Col. 4-6, section 0017-0019, fig. 3, unit 21111, fig. 4, unit 21120) with each row of the array and for accumulating counts of voltage levels of the binary pulses occurring at the time offsets of the bit stream during a duration time when the pulse voltage levels are within the voltage threshold window at each row and column point of the array and displaying the array column and row points of the accumulated time and voltage counts as an eye diagram defining characteristics of the bit stream of binary pulses (fig. 2, 203, 200, 214, 3, fig. 3, unit 21113-21117, fig. 5, 6).

Regarding claim 8:

Thomas Eugene, James Roger, Robert Lee disclose apparatus for measuring characteristics of a bit stream of binary pulses comprising first control means for defining a window comparator of an array of columns and rows defining points for accumulating event counts at time offsets during defined duration times of the binary pulse bit stream, second control means for creating a voltage threshold window that moves between a minimum and maximum voltage threshold with each row of the array, logic means for detecting voltage levels of the binary pulses occurring at time offsets of the bit stream when the pulse voltage levels are within the voltage threshold at each row and column point of the array (fig. 2,

203, 200, 214, 3, fig. 3, unit 21113-21117, fig. 5, 6), first counter means for accumulating counts of the detected binary pulse voltage levels at time offsets during each defined duration time of the binary pulse bit stream in a column and row point of the array (fig. 2, 203, 200, 214, 3, fig. 3, unit 21113-21117, fig. 5, 6), second counter means for determining duration of periods of the binary bit stream in which to accumulate the detected binary pulse voltage levels at each point of ; the array, and monitor apparatus for displaying the array column and row points of the accumulated event counts as an eye diagram defining characteristics of the bit stream of binary pulses (fig. 2, 203, 200, 214, 3, fig. 3, unit 21113-21117, fig. 5, 6).

Regarding claim 9:

Thomas Eugene, James Roger, Robert Lee disclose a method for determining characteristics of a bit stream of binary pulses comprising the steps of defining a window comparator, and accumulating various voltage counts (Col. 4-6, section 0017-0019, fig. 3, unit 21113, 21114-21117) of the bit stream pulses at time offsets during defined duration times of the binary pulse bit stream within voltage threshold at points inside the window comparator and drawing an eye diagram therefrom defining the bit stream pulse characteristics (fig. 2, 203, 200, 214, 3, fig. 3, unit 21113-21117, fig. 5, 6, Col. 4-6, section 0017-0019).

Regarding claim 15:

Thomas Eugene, James Roger, Robert Lee disclose a method for determining characteristics of a bit stream of binary pulses comprising the steps of defining a

window comparator of an array of columns and rows defining points for accumulating event counts of the binary pulse bit stream at time offsets during defined durations of the binary pulse bit stream creating a voltage threshold window that moves between a minimum voltage and a maximum voltage at each row of the array (Col. 4-6, section 0017-0019, fig. 3, unit 21113, 21114-21117) and accumulating counts of voltage levels of the binary pulses occurring at time offsets of the bit stream during a duration time when the pulse voltage levels are within the voltage threshold window at each row and column point of the array and displaying the array column and row points of the accumulated event counts as an eye diagram defining characteristics of the bit stream of binary pulses (fig. 3, unit 21119-21118, fig. 4, unit 21121-21127, fig. 5, 6).

Regarding claim 16:

Thomas Eugene, James Roger, Robert Lee disclose a method for determining characteristics of a bit stream of binary pulses comprising the steps of defining a window comparator of an array of columns and rows defining points for accumulating event counts at time offsets during defined duration times of the binary pulse bit stream creating a voltage threshold window that moves between defined voltage levels at each row of the array detecting voltage levels of the binary pulses occurring at the time of the bit stream when the pulse voltage levels are within the voltage threshold window at each row and column point of the array accumulating counts of the detected binary pulse voltage levels at the time offsets in a column and row point of the array and displaying the array

column and row points of the accumulated time and voltage counts as an eye diagram defining characteristics of the bit stream of binary pulses (fig. 2, 203, 200, 214, 3, fig. 3, unit 21113-21117, fig. 5, 6).

Regarding claims 2, 3, 4, 5, 6, 10-14:

Thomas Eugene, James Roger, Robert Lee disclose the level of voltage is programmable of the array (fig. 3, unit 21110-21118, fig. 4, unit 21120-21127); using threshold voltage windows (fig. 3, unit 21110-21118, fig. 4, unit 21120-21127); using counter means for the stream (fig. 2, unit 203, 211; fig. 3, unit 21110-21118, fig. 4, unit 21120-21127); displaying array (fig. 2, unit 3, fig. 5, 6), accumulating counts, offset value (fig. 2, unit 3, fig. 5, 6, fig. 3, unit 21110-21118, fig. 4, unit 21120-21127).

Response to Arguments

2. Applicant's arguments filed 07/12/2005 have been fully considered but they are not persuasive.

A. Applicant argues in the arguments that the prior art does not show 'accumulating time and voltage counts of the bit stream pulses falling within voltage thresholds and points inside the window comparator during durations of the binary pulse bit stream'. Thomas Eugene, James Roger, Robert Lee disclose 'accumulating time and voltage counts of the bit stream pulses (fig. 2, unit 203, 200) falling within voltage thresholds and points inside the

window comparator during durations of the binary pulse bit stream' in fig. 2, unit 200, 203, 20, 3, fig. 3, unit 21111, fig. 4, unit 21120.

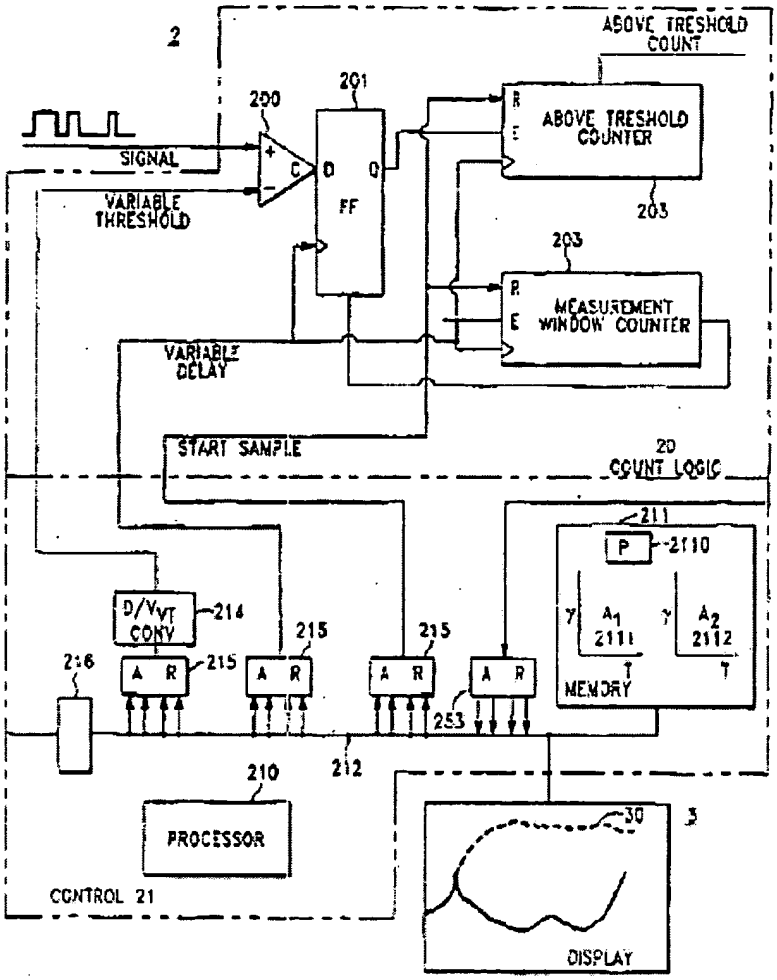

FIG.-2

B. Applicant continues to argue in the arguments that the prior art does not show 'minimum and maximum voltage level', Thomas Eugene, James Roger, Robert Lee disclose 'minimum and maximum voltage level' in fig. 3, unit 21113 and 21117.

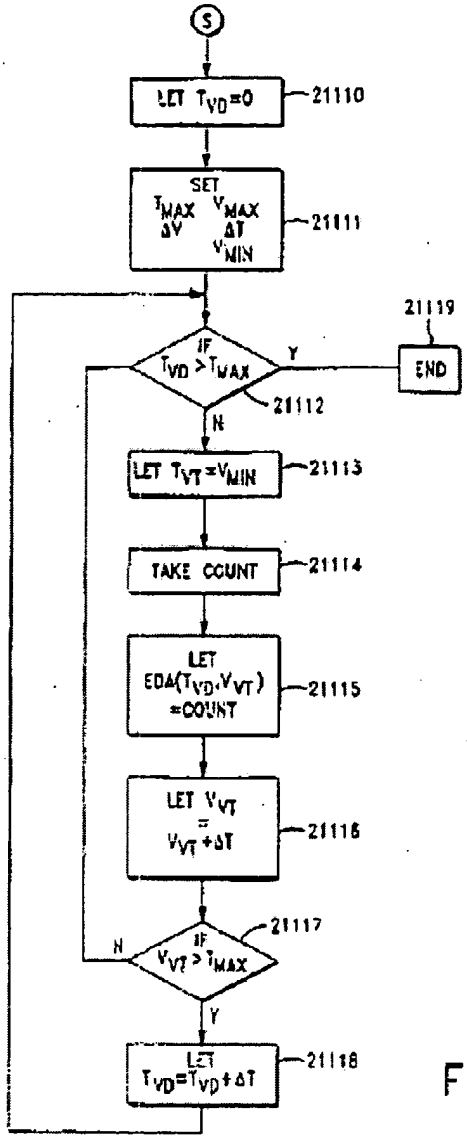

FIG.—3

C. Applicant continues to argue in the arguments that the prior art does not show 'voltage windows' and cited paragraph 19, line 1-7 as evidence.

First Thomas Eugene, James Roger, Robert Lee disclose 'voltage windows' in fig. 1, unit 203, 200, 201. Second, in paragraph 19, line 1-7 talks about a 1 bit comparator connecting to a d-flip flop, not sure how the applicant interprets a 1 bit comparator connecting to a d flip-flip has no 'voltage windows', in fact, on line 5-48 of paragraph 19, it talks about use of a d flip-flip continuously with q output with a threshold windows comparator counter which is a 'voltage windows' with a Vmax and Vmin to produce an eye diagram in fig. 6.

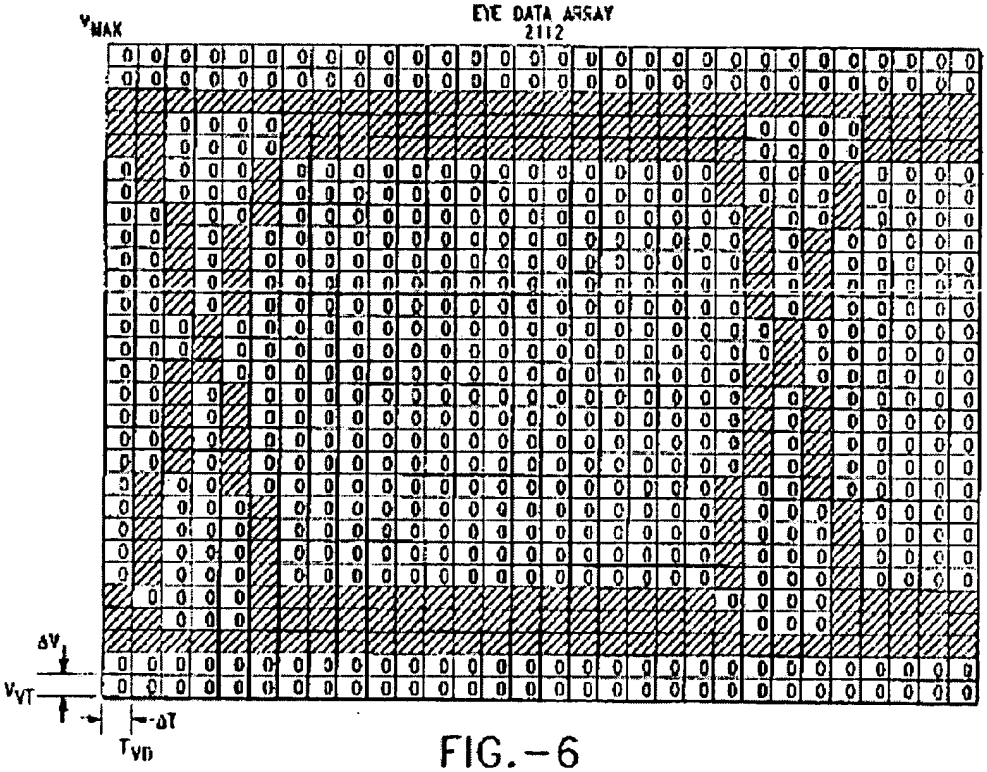

FIG.-6

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tung S Lau whose telephone number is 571-272-2274. The examiner can normally be reached on M-F 9-5:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on 571-272-2269. The fax phone numbers for the organization where this application or proceeding is assigned is 703-872-9306

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TL

MICHAEL NGHIEM
PRIMARY EXAMINER